

## 2011/Fall Computer Architecture PhD Qualifying Exam

\* Answer each question in 10 lines or you will be given penalty points.

**1. Three enhancements with the following speedups are proposed for a new architecture.**

**Speedup<sub>1</sub>=30 speedup<sub>2</sub>=20 speedup<sub>3</sub> = 10.**

**Only one enhancement is usable at a time. Assume the enhancements can be used 25%, 35%, and 15% of the time for enhancements 1, 2, and 3, respectively. For what fraction of the “reduced execution time”, not the “original execution time”, is no enhancement used? (20points)**

**2. To reduce branch instruction related cycle penalty in pipelined architectures, we need to know branch outcomes and branch target addresses early in the pipeline. How can you do that? (10points) Explain recent architectural methods/schemes for that (10points).**

**3. What are reservation stations used in the Tomasulo algorithm? (10points) How are registers renamed in the Tomasulo algorithm? (10points)**

**4. Memory hierarchy (20points).**

**(a) Compare and contrast the roles of L1 and L2 caches? (8points)**

**(b) Miss penalties of replacing all cache lines in write back caches are the same (true or false) and why? (7points).**

**(c) How can you reduce write traffic to memory in write-through caches? (7points)**

**5. What is snooping in multiprocessors? (8points) How can you implement snooping? (7points) What are the problems or disadvantages of snooping? (7points)**