2014/Spring Computer Architecture PhD Qualifying Exam

Student ID _____   Name _____

* Answer each question in *10 lines* <u>or you will be given penalty points</u>.

1. To reduce branch instruction-related cycle penalty in pipelined architectures, we need to know branch outcomes and branch target addresses early in the pipeline. How can you do that? Explain recent architectural methods/schemes for that (25 points).

2. What is the key hardware structure of the speculative Tomasulo algorithm, compared to original Tomasulo algorithm? Explain its roles (25 points).

3. Memory hierarchy (25 points)
(a) Explain write-allocate and write-no-allocate policies.
(a) What is the merging write buffer?

4. What is snooping in multiprocessors? Explain what will occur when a memory block is in the modified (exclusive) state and a processor node incurs a write miss in the memory block in snooping-based MSI multiprocessor systems (25 points).

1. 최상 20, 중상 16, 중 12, 중하 8, 하 4, 최하 0

2. branch prediction or early branch outcome resolution, generate target address early
각각 **5점**
BTB, 1-bit 2-bit branch predictors, 2-level predictors.
각각 **5점**

3. Determine data dependency among instructions and issue them out-of-order and dynamically. Remove name dependencies using register renaming. When register values are ready, register numbers are replaced with those values in reservation stations. Otherwise, they are renamed to the reservation station number which will provide those values.

4. (a) L1: fast (4점) L2: low miss rate (4점)

(b) False(3점) dirty lines require replacing dirty data back to memory(4점)

(c) via write buffer(3점) which merges writes to the same lines and sends memory requests when no reads(4점)

5. (a) checking bus for incoming data or invalidation request
(b) each cache controller checks all memory transactions on the bus
(c) scalability with increasing number of nodes on the bus

Student1 48
Student2 71
Student3 86
Student4 65
Student5 69
Student6 31